Preliminary Data Sheet PD60185-C

International
IOR Rectifier

# IR1176

## SYNCHRONOUS RECTIFIER DRIVER

### Features

- Provides constant and proper gate drive to power MOSFETs regardless of transformer output
- Minimizes loss due to power MOSFET body drain diode conduction
- Stand alone operation - no ties to primary side
- Schmitt trigger input with double pulse suppression allows operation in noisy environments
- High peak current drive capability - 4A
- High speed operation - 2MHz
- Adaptable to multiple topologies

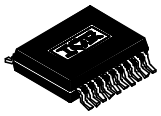
### Product Summary

| | |
|---|---|
| $V_{dd}$ | 5Vdc |
| $I_{O+/-}$ (peak) | 4A/4A |
| $F_{max}$ | 2MHz |
| Max lead time | 500nsec |

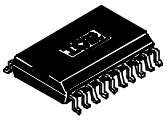
### Description

The IR1176 is a high speed CMOS controller designed to drive N-channel power MOSFETs used as synchronous rectifiers in high current, high frequency forward converters with output voltages equal or below 5$V_{DC}$. Schmitt trigger inputs with double pulse suppression allow the controller to operate in noisy environments. The circuit does not require any ties to the primary side and derives its operating power directly from the secondary. The circuit functions by anticipating transformer output transitions, then turns the power MOSFETs on or off before the transitions of the transformer to minimize body drain diode conduction and reduce associated losses. Turn on/off lead time can be adjusted to accommodate a variety of power MOSFET sizes and circuit conditions. The IR1176 also provides gate drive overlap/dead-time control via external components to further minimize diode conduction by nulling effects of secondary loop and device package inductance.

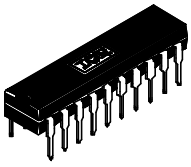
### Packages



**IR1176S**
20 Lead Surface Mount
(SSOP-20)



**IR1176SS**
20 Lead SOIC (MS-013AC)



**IR1176**
20 Lead PDIP
(MS-001AD)

## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur.

| Symbol | Definition | | Min. | Max. | Units |
|---|---|---|---|---|---|
| $V_{dd}$ | Supply voltage | | — | 7 | $V_{DC}$ |
| $I_{in}$ | Input clamp current | | — | +/- 10 | $mA_{DC}$ |
| $P_D$ | Power dissipation | (SSOP-20) | — | 400 | mW |
| | | (SOIC) | — | — | — |
| | | (PDIP) | — | — | — |
| $Rth_{JC}$ | Thermal resistance | (SSOP-20) junction-to-case | — | 28.5 | °C/W |
| | | (SOIC) junction-to-case | — | 20 | |
| | | (PDIP) junction-to-case | — | 28.1 | |
| $Rth_{JA}$ | Thermal resistance | (SSOP-20) junction-to-ambient | — | 90.5 | |
| | | (SOIC) junction-to-ambient | — | 45 | |
| | | (PDIP) junction-to-ambient | — | 62.4 | |
| $T_J$ | Junction temperature | | — | 150 | °C |
| $T_S$ | Storage temperature | | -55 | 150 | |
| $T_L$ | Lead temperature (soldering, 10 seconds) | | — | 300 | |

## Recommended Operating Conditions

| Symbol | Definition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Vdd | Supply voltage operating range | — | 5 | — | $V_{DC}$ |
| $T_A$ | Ambient temperature | −40 | — | 85 | °C |
| Freq | Operating frequency | 250 | — | 500 | KHz |
| Rbias | Required bias resistor (+/- 1%) | — | 34.0 | — | KΩ |
| UV | Voltage at UVSET pin | 1.75 | — | 2.25 | $V_{DC}$ |
| Xin | Maximum voltage at X1 and X2 inputs | — | — | 5.6 | $V_{DC}$ |
| Cd1/Cd2 | Capacitance at pins DTIN1 and DTIN2 | — | — | 100 | pF |

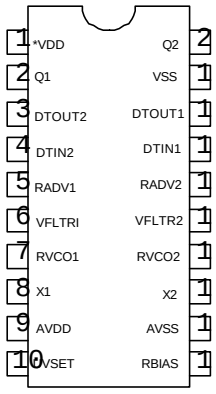
## Dynamic Electrical Characteristics

Vdd=5V, $T_A$ = 25°C, Rbias = 34.0K unless otherwise specified.

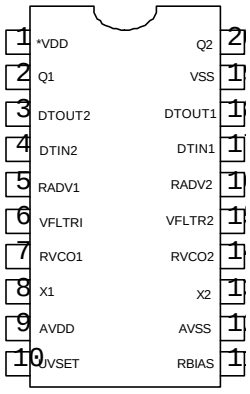
| Symbol | Definition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Vdd | Supply voltage operating range | 4.0 | — | 5.25 | $V_{DC}$ |
| Iqdd | Vdd quiescent current (x1 = x2 = 0V or 5V, Iout = 0) | — | 4 | 5 | A |
| Freq | Operating frequency | 100 | — | 2000 | KHz |
| UVSET+ | UVSET positive going threshold | 1.10 | — | 1.4 | V |
| UVSET- | UVSET negative going threshold | 0.8 | — | 1.1 | V |
| Vxth+ | X1/X2 Input positive going threshold | — | 1.4 | — | $V_{DC}$ |
| Vxth- | X1/X2 Input negative going threshold | — | 1.0 | — | $V_{DC}$ |
| Tadv | Externally adjustable lead time (advance) | — | — | 500 | nsec |
| Td | Externally adjustable dead-time for Q1 and Q2 | 20 | — | — | nsec |
| Isink (peak) | Q1,Q2 output sink current (Vdd=5.0V, pulsed, 10 usec) | — | 4 | — | A |
| Isource (peak) | Q1,Q2 output source current (Vdd=5.0V, pulsed, 10 usec) | — | 4 | — | |
| VOH | Q1, Q2 High level voltage (Iout = 20mA) | — | Vdd- 0.20 | — | V |
| VOL | Q1, Q2 Low level voltage (Iout = 20mA) | — | 0.10 | — | |
| tio | Input to output delay (PLL bypassed, cross coupled mode) | — | 20 | — | nsec |
| tr | Gate turn-on rise time (C1=1000pf, Vdd=5V) | — | 20 | — | nsec |
| tf | Gate turn-off fall time (C1=1000pf, Vdd=5V) | — | 20 | — | nsec |
| Vtr | Cross-over voltage (Vdd=5Vdc, DTIN shorted to DTOUT, C1=1000pf) Fig. 3 | — | 2.5 | — | $V_{DC}$ |
| Rbias | Required bias resistor (1%) | — | 34.0 | — | KΩ |
| Vbias | Voltage at Rbias pin | — | 1.25 | — | $V_{DC}$ |
| Tjitter | Phase-lock loop output jitter | -20 | — | 20 | nsec |
| Ichgpump | Charge pump output current (at VFLTR pin) | — | 50 | — | $\mu A_{DC}$ |
| Vchgpump | Charge pump output voltage (at VFLTR pin) | 1.3 | 1.5 | 1.7 | $V_{DC}$ |
| Kvco_dc | PLL Vco DC gain (per design) | — | 62 | — | KHz/ Volt |

## Lead Definitions and Assignments

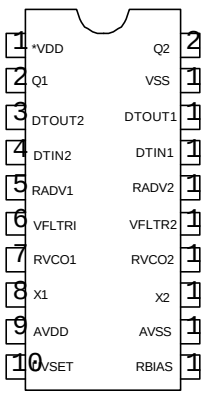
| Symbol | Description |
|---|---|
| AVDD | Power - + 5 $V_{DC}$ to MOSFET drivers |
| Q1 | Output - gate drive for Q1 power MOSFET |
| DTOUT1 | Output - sets dead time for Q1 output - used with DTIN1 |
| DTIN1 | Input - sets dead time for Q1 - used with DTOUT1 |
| RADV1 | Output - sets lead time (advance) for Q1 |
| VFLTR1 | Output - PLL loop filter for Q1 output |
| RVCO1 | Output - sets PLL center frequency for Q1 output |
| X1 | Input - transformer input for Q1 |
| VDD | Power - +5 Vdc for internal logic |
| UVSET | Input - sets UVLO+ If this pin is pulled below 1.25VDC externally, then both Q1 and Q2 outputs will be at Vss (disabled) |
| RBIAS | Output - connected to 34.0K +/- 1% resistor - sets operating current |
| AVSS | Ground for MOSFET driver supply (VDD) |
| X2 | Input - transformer input for Q2 |
| RVCO2 | Output - sets PLL center frequency for Q2 output |
| VFLTR2 | Output - PLL loop filter for Q2 |
| RADV2 | Output - sets lead time (advance) for Q2 |
| DTIN2 | Input - sets dead time for Q2 - used with DTOUT2 |
| DTOUT2 | Output - sets dead time for Q2 - used with DTIN2 |
| VSS | Ground for logic supply (AVDD) |
| Q2 | Output - gate drive for Q2 power MOSFET |




**IR1176S**
(SSOP-20)




**IR1176SS**
**SOIC (wide body)**




**IR1176**
**PDIP**

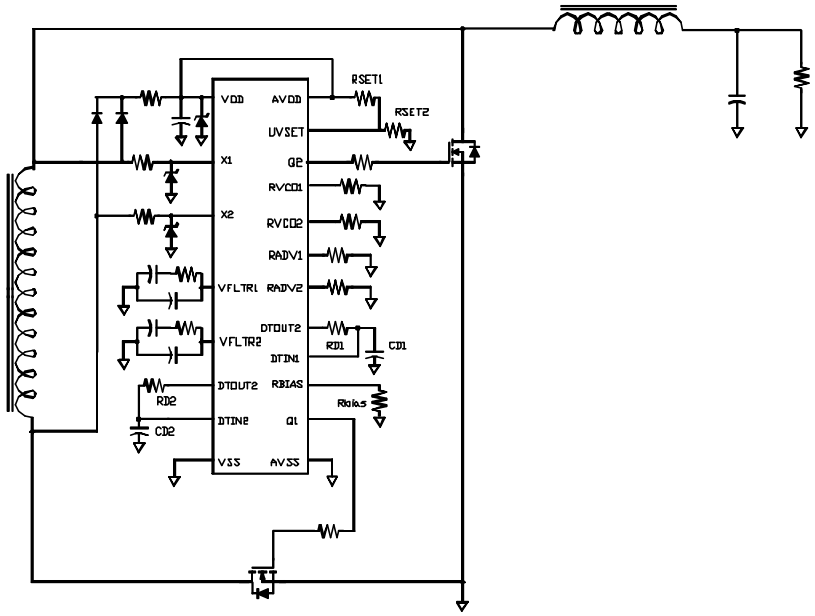



**Fig. 1 Typical application circuit when supply Vout < 5.0 $V_{DC}$**

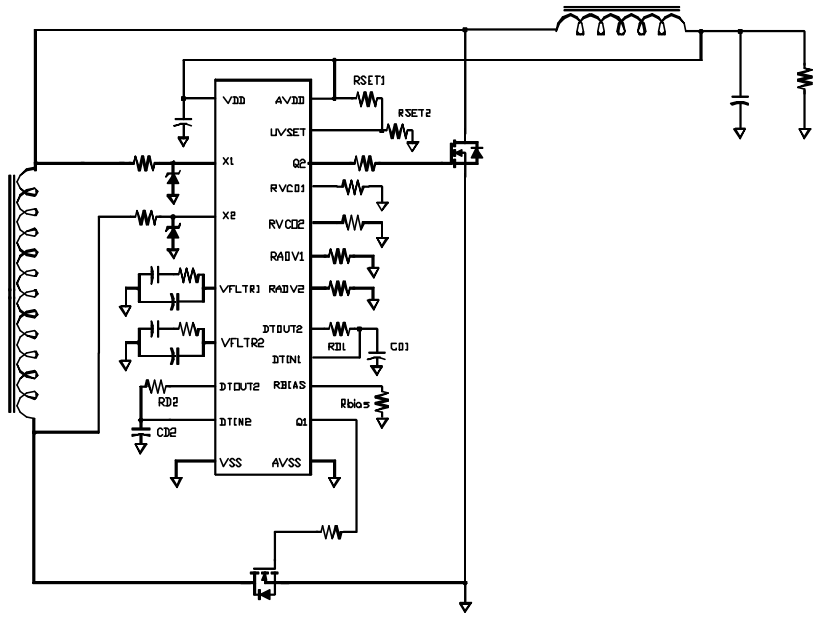



**Fig. 2 Typical application circuit when supply Vout = 5.0 $V_{DC}$**

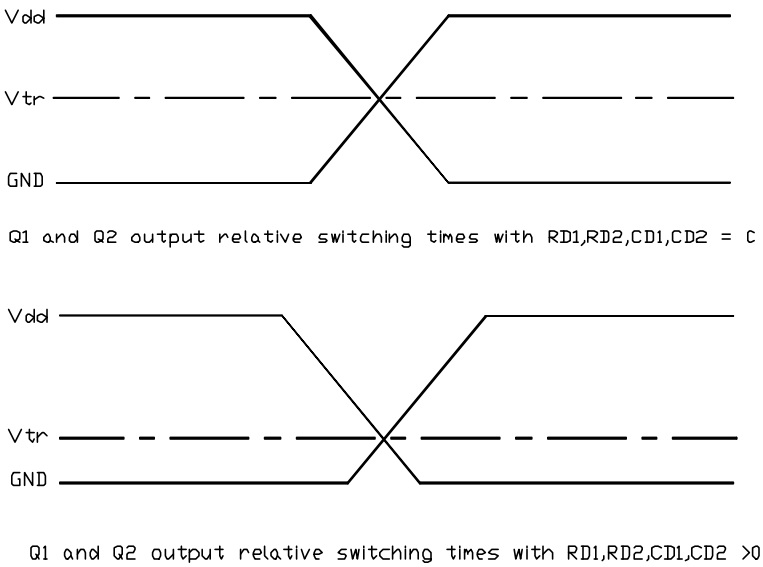



**Fig. 3 Gate drive characteristics and definitions**

## Phase Lock Loop Design Equations:

1 - Resistor to set VCO Ceter Frequency:

**Rvco (KΩ) = [1E2 x Vchgpump($V_{DC}$) / fvco(KHz)] x Kvco _ dc(KHz/Volt)**

Example (A): Choose Vchgpump = 1.5V, desired frequency (fvco) = 300KHz

Rvco = [1E2 x 1.5 /300] x 62 Hz = 31 KΩ

2 - Small Signal gain for VCO:

**Kvco_ac (KHz/Volt) = 1E2 x Kvco_dc (KHz/Volt)/Rvco(KΩ)**

Example (B): Choosing same conditions as in example A:

Kvco_ac = 1E2 x 62 / 31 = 200 KHz/volt

3 -PLL Natural frequency:

$$wn = 2pfn(KHz) = \sqrt{Ichpump(uA) \times Kvco\_ac(KHz/V) / C(nF)}$$

Choose Cf such that **Cf=C/16**

4 -PLL Damping factor calculations:

$$P = pE\text{-}3 \times Rf(KOhms) \times C(nF) \times fn(KHz)$$

Typical value for P is 0.707. (Critically damped)

5 -Advance timing:

$$Tadv(nsec) = RADV(KOhms)*10 + 6$$

Where RADV is resistance from RADV1 or RADV2 to ground.
Example C:RADV=10Kohms will result in Tadv=10*10+ 6=106 nsec.

6-Dead time calculations:

$$Td(nsec) = 0.69*Cdt(pF)*(Rdt(K\Omega)+0.15) \text{ (For Vdd=5V)}$$

Where Rdt is resistance between pins DTIN1 and DTOUT1 or DTIN2 and DTOUT2. Cdt is capacitance from DTIN1 or DTIN2 to ground.
Example D: Rd=2KW and Cdt=100pF will result in Td=148.35nsec.

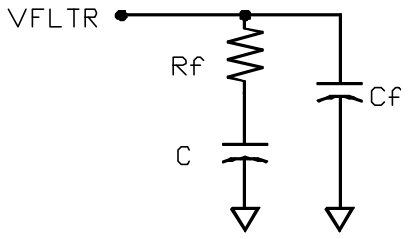



**Fig. 4 PLL loop filter component definitions**

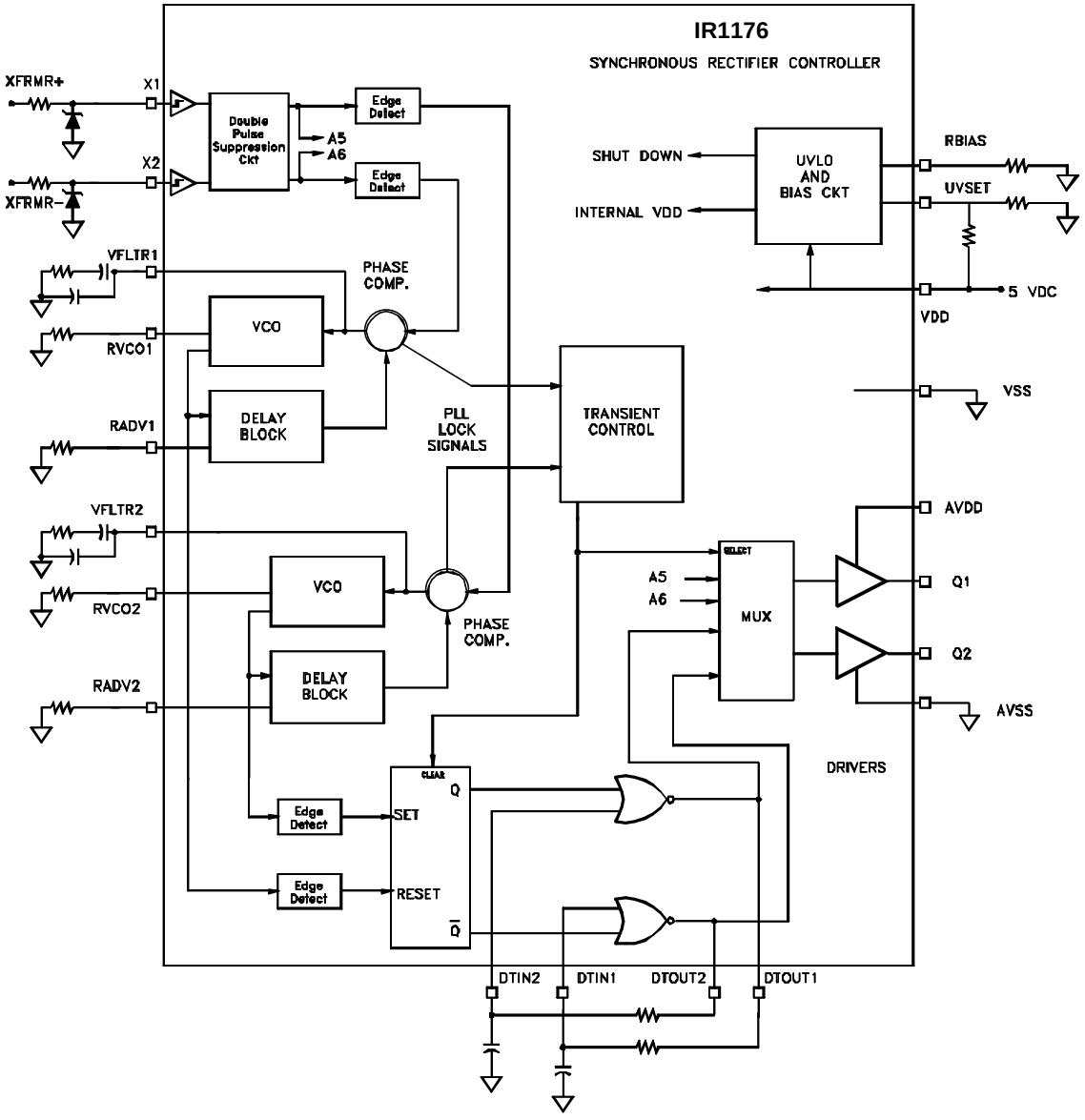
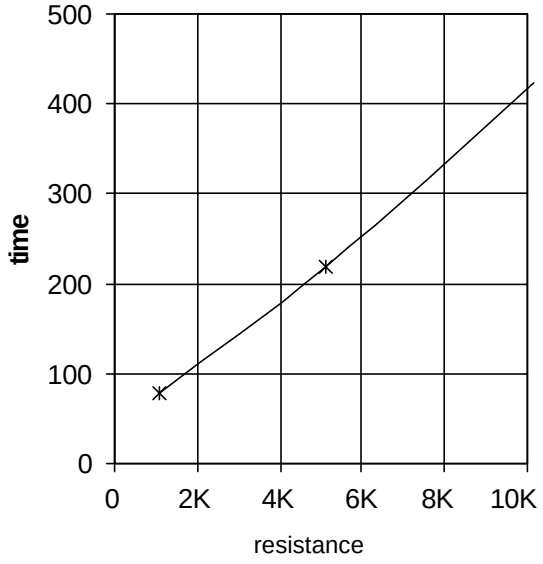
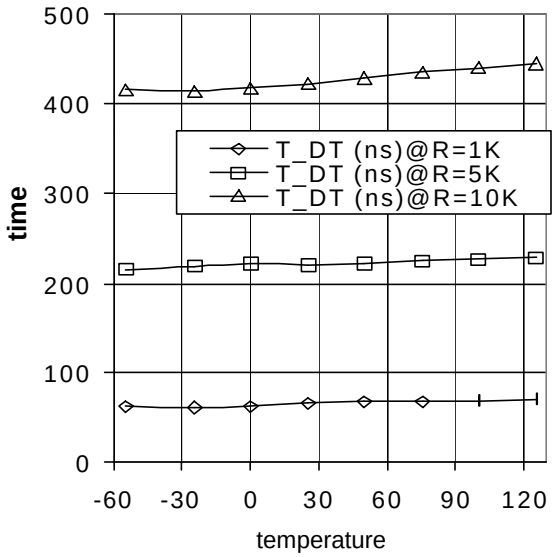


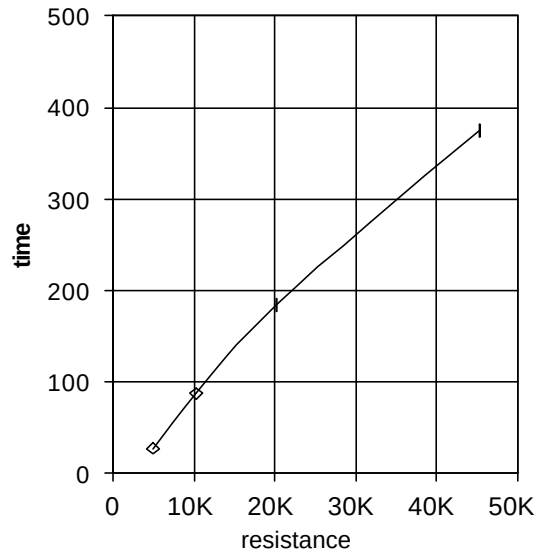

**Fig. 5 IR1176 Block Diagram**



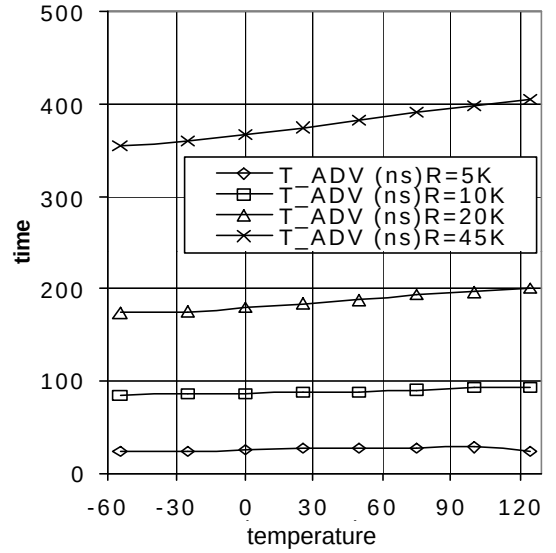

Response at 25°C
**T_DT vs R_DT, C = 100pF**




Temperature Response
**T_DT vs R_DT, C = 100pF**

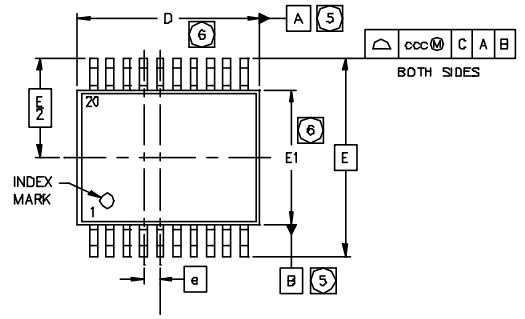


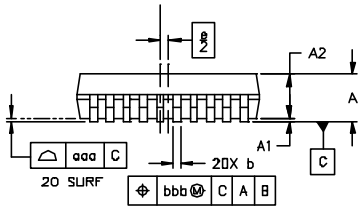

Response at 25°C
**T_ADV vs R_ADV**

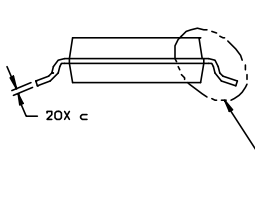


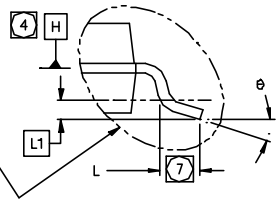

Temperature Response
**T_ADV vs R_ADV**

## Case Outline




| SYMBOL | MO-150AE DIMENSIONS | | | | | |
|---|---|---|---|---|---|---|
| | MILLIMETERS | | | INCHES | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | --- | 2.00 | --- | --- | .078 |
| A1 | 0.05 | --- | --- | .002 | --- | --- |
| A2 | 1.65 | 1.75 | 1.85 | .065 | .069 | .072 |
| b | 0.22 | --- | 0.38 | .009 | --- | 014 |
| c | 0.09 | --- | 0.25 | .004 | --- | .009 |
| D | 6.90 | 7.20 | 7.50 | .272 | .283 | .295 |
| E | 7.80 BSC | | | .307 BSC | | |
| E1 | 5.00 | 5.30 | 5.60 | .197 | .209 | .220 |
| e | 0.65 BSC | | | 026 BSC | | |
| L | 0.55 | 0.75 | 0.95 | .022 | .029 | .037 |
| L1 | 0.25 BSC | | | .010 BSC | | |
| θ | 0° | 4° | 8° | 0° | 4° | 8° |
| aaa | 0.10 | | | .004 | | |
| bbb | 0.15 | | | .006 | | |
| ccc | 0.20 | | | .008 | | |

NOTES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.

(4) DATUM PLANE H IS LOCATED AT THE MOLD PARTING LINE.

(5) DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.

(6) DIMENSIONS D AND E1 DO NOT INCLUDE PROTRUSIONS AND ARE MEASURED AT DATUM PLANE H. PROTRUSIONS SHALL NOT EXCEED 0.20 [.008] PER SIDE

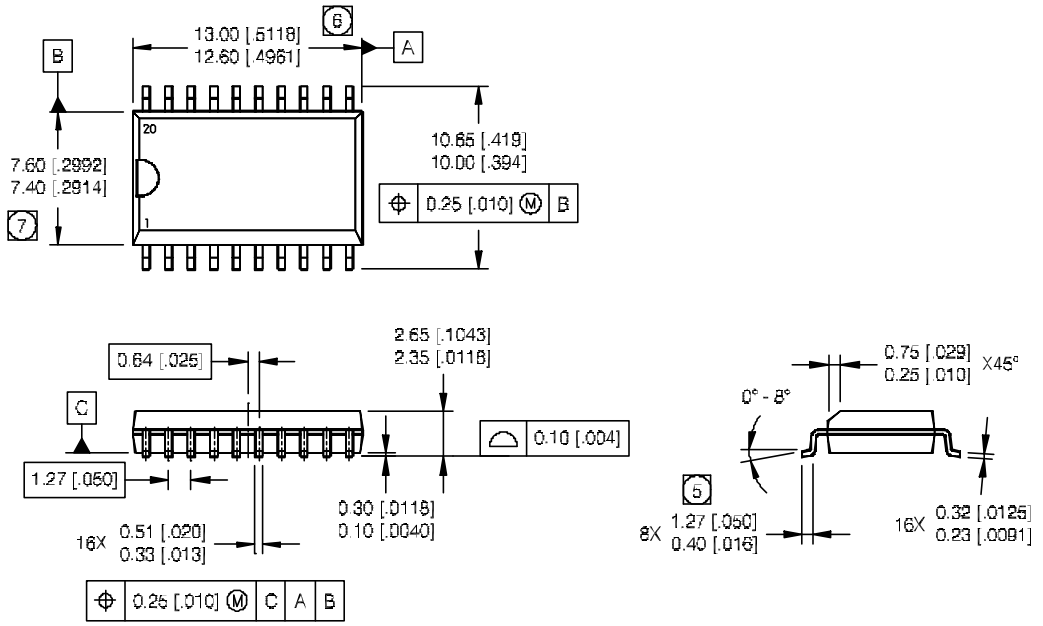
(7) DIMENSION L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE.

8 OUTLINE CONFORMS TO JEDEC OUTLINE MO-150AE.

**20 Lead Surface Mount (SSOP-20)**

01-6057 00
01-3078 00 (MS013AC)

## Case Outline




NOTES.

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AC.

5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

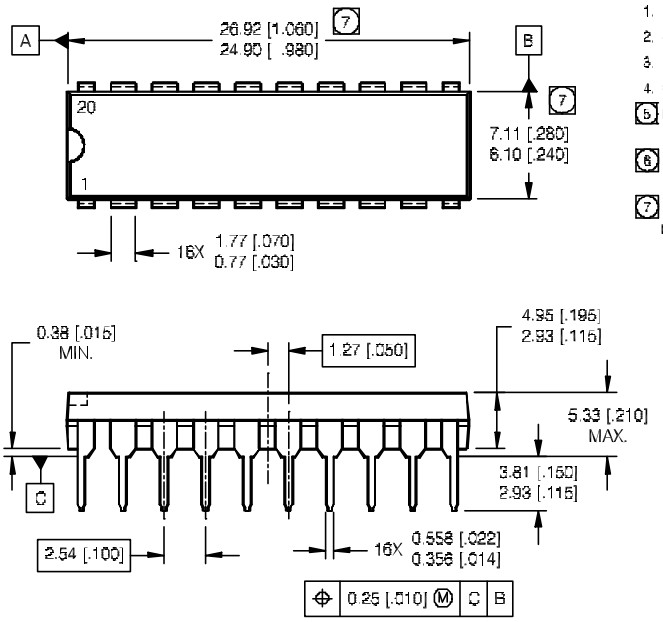
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS.
MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

7 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS.
MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

**20 Lead SOIC**

01-6070 00
01-3080 00 (MS013AC)

## Case Outline



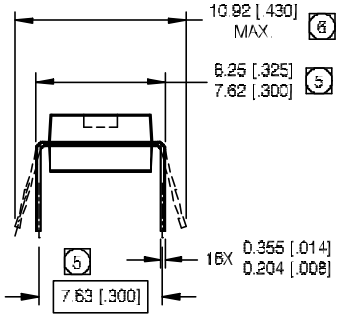

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AD.

(5) DIMENSION MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C

(6) DIMENSION MEASURED AT LEAD TIPS WITH THE LEADS UNCONSTRAINED.

(7) DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS
MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].




**20 Lead PDIP**

01-6069 00
01-3079 00 (MS001AD)